

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the above-referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A chip-scale package, comprising:
a semiconductor device including an active surface; and
a substrate comprising a semiconductor material disposed adjacent said the active surface and including:
at least one electrically conductive via extending at least partially therethrough,
positioned over said the semiconductor device, and in communication with a corresponding bond pad of said the semiconductor device; and
at least one conductive trace in communication with said the at least one electrically conductive via and carried on a surface of said the substrate which is opposite from another surface of said the substrate that is adjacent to said the semiconductor device.

2. (Currently amended) The chip-scale package of claim 1, further comprising an electrically conductive bump protruding from said the substrate opposite said the semiconductor device and, in communication with said the at least one electrically conductive via, and located at an opposite end of the at least one conductive trace from the at least one electrically conductive via.

3. (Currently amended) The chip-scale package of claim 1, wherein said the substrate comprises at least another electrically conductive via that extends substantially directly therethrough.

4. (Canceled)

5. (Currently amended) The chip-scale package of claim 1, wherein a substrate of said the semiconductor device and said the substrate comprising semiconductor material comprise the same type of semiconductor material.

6. (Currently amended) The chip-scale package of claim 1, wherein a substrate of said the semiconductor device and said the substrate comprising semiconductor material comprise materials having substantially the same coefficients of thermal expansion.

7. (Currently amended) The chip-scale package of claim 1, wherein a substrate of said the semiconductor device comprises silicon.

8. (Currently amended) The chip-scale package of claim 1, wherein said the semiconductor material comprises silicon.

9. (Currently amended) The chip-scale package of claim 1, wherein a first thickness of said the semiconductor device and a second thickness of said the substrate are substantially the same.

10. (Currently amended) The chip-scale package of claim 1, wherein a first thickness of said the semiconductor device is greater than a second thickness of said the substrate.

11. (Currently amended) The chip-scale package of claim 1, wherein said the another surface of said the substrate is at least partially coated with an insulative material.

12. (Currently amended) The chip-scale package of claim 11, wherein said the insulative material comprises a layer extending substantially over said the surface.

13. (Currently amended) The chip-scale package of claim 11, wherein said the insulative material comprises an oxide.

14. (Currently amended) The chip-scale package of claim 11, wherein said the insulative material comprises silicon oxide.

15. (Currently amended) The chip-scale package of claim 1, further comprising an intermediate layer disposed between said the semiconductor device and said the substrate.

16. (Currently amended) The chip-scale package of claim 15, wherein said the intermediate layer comprises an adhesive material.

17. (Currently amended) The chip-scale package of claim 15, wherein said the intermediate layer comprises polyimide.

18. (Currently amended) The chip-scale package of claim 15, wherein said the at least one electrically conductive via and said the corresponding bond pad communicate through said the intermediate layer.

19. (Currently amended) The chip-scale package of claim 1, wherein conductive material of said the at least one electrically conductive via is bonded to said the corresponding bond pad.

20. (Currently amended) The chip-scale package of claim 1, wherein a contact between said the at least one electrically conductive via and said the corresponding bond pad comprises a diffusion region comprising a bond pad material and a via material.

21. (Currently amended) A chip-scale package, comprising:
a substrate comprising semiconductor material and including:
a first surface with contact areas arranged correspondingly to an arrangement of bond pads on an active surface of a semiconductor device of the chip-scale package; conductive vias extending therethrough and corresponding to said the contact areas; and a second surface carrying at least one conductive trace extending laterally from a conductive via of said the conductive vias; and
said the semiconductor device invertedly disposed adjacent said the substrate so that bond pads of said the semiconductor device communicate through with corresponding conductive vias of said the substrate.

22. (Currently amended) The chip-scale package of claim 21, wherein said the bond pads contact said the corresponding conductive vias.

23. (Currently amended) The chip-scale package of claim 22, further comprising diffusion regions between said the bond pads and said the corresponding conductive vias.

24. (Currently amended) The chip-scale package of claim 23, wherein each of said the diffusion regions comprises a bond pad material and a via material.

25. (Currently amended) The chip-scale package of claim 24, wherein said the diffusion regions at least partially secure said the semiconductor device to said the substrate.

26. (Currently amended) The chip-scale package of claim 21, further comprising an intermediate layer disposed between said the substrate and said the semiconductor device.

27. (Currently amended) The chip-scale package of claim 26, wherein said the bond pads and said the corresponding vias contact each other through said the intermediate layer.

28. (Currently amended) The chip-scale package of claim 26, wherein said the intermediate layer comprises a material which adheres said the semiconductor device to said the substrate.

29. (Currently amended) The chip-scale package of claim 26, wherein said the intermediate layer comprises a polyimide.

30. (Currently amended) The chip-scale package of claim 21, further comprising at least one conductive bump in communication with at least one conductive via of said the corresponding conductive vias and, protruding from said the substrate opposite from said the semiconductor device, and located at an opposite end of the at least one conductive trace from the at least one conductive via.

31. (Currently amended) The chip-scale package of claim 30, wherein said the at least one conductive bump comprises solder.

32. (Currently amended) The chip-scale package of claim 21, wherein said the substrate comprising semiconductor material and a substrate of said the semiconductor device comprise the same material.

33. (Currently amended) The chip-scale package of claim 21, wherein said the substrate comprises silicon.

34. (Currently amended) The chip-scale package of claim 21, wherein a substrate of said the semiconductor device comprises silicon.

35. (Currently amended) The chip-scale package of claim 21, wherein a first thickness of said the substrate and a second thickness of said the semiconductor device are substantially equal.

36. (Currently amended) The chip-scale package of claim 21, wherein a first thickness of said the substrate is less than a second thickness of said the semiconductor device.

37. (Currently amended) The chip-scale package of claim 21, further comprising an insulative material disposed on at least a portion of said the second surface of said the substrate.

38. (Currently amended) The chip-scale package of claim 37, wherein at least one conductive via of said the corresponding conductive vias is exposed through said the insulative material.

39. (Currently amended) The chip-scale package of claim 37, wherein said the insulative material comprises an oxide.

40. (Currently amended) The chip-scale package of claim 37, wherein said the insulative material comprises silicon oxide.

41. (Currently amended) The chip-scale package of claim 37, wherein said the insulative material comprises an insulative layer disposed substantially over said the second surface.

42. (Canceled)

43. (Currently amended) A flip-chip carrier, comprising a substrate comprising semiconductor material and including:

at least one via formed therethrough and having a first end located proximate a first surface of said the substrate and positioned to substantially align with a corresponding bond pad of a semiconductor device to be assembled with said the substrate; and

at least one conductive trace laterally extending from a second end of said the at least one via and carried by a second surface of said the substrate.

44. (Currently amended) The flip-chip carrier of claim 43, wherein said the at least one via comprises an electrically conductive material.

45. (Currently amended) The flip-chip carrier of claim 43, further comprising an insulative material disposed on at least a portion of at least one surface of said the substrate.

46. (Currently amended) The flip-chip carrier of claim 45, wherein said the insulative material comprises an oxide.

47. (Currently amended) The flip-chip carrier of claim 45, wherein said the insulative material comprises silicon oxide.

48. (Currently amended) The flip-chip carrier of claim 45, wherein said the insulative material comprises an insulative layer disposed substantially over said the at least one surface.

49. (Currently amended) The flip-chip carrier of claim 45, wherein said the at least one via is exposed through said the insulative material.

50. (Currently amended) The flip-chip carrier of claim 43, wherein said the substrate comprises silicon.

51. (Currently amended) The flip-chip carrier of claim 43, further comprising a conductive bump disposed adjacent an end of said the at least one conductive trace located opposite from said the second end of said the at least one via.

52. (Currently amended) The flip-chip carrier of claim 51, wherein said the conductive bump comprises solder.

53. (Currently amended) The flip-chip carrier of claim 43, further comprising an adhesive layer disposed adjacent said the first surface of said the substrate.

54. (Currently amended) The flip-chip carrier of claim 53, wherein said the adhesive layer comprises a polyimide.

55. (Currently amended) The flip-chip carrier of claim 53, wherein said the first end of said the at least one via extends through said the adhesive layer.

56-72. (Canceled)